**EXAMINER'S AMENDMENT**

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Hanke (reg. on 58,076).

The application has been amended as follows:

1. (Currently Amended) A graphics rendering engine stored on ~~a computer-storage medium~~ memory and executable by a computer, the graphics rendering engine comprising:

source code represented as a first sequence of instruction addresses for display upon a screen accessible to a user, wherein the screen comprises a graphical user interface (GUI) for receiving user input to select one of the instruction addresses;

a sequence of processor pipeline stages attributable to respective ones of the instruction addresses, wherein ~~during times when the user input is received by the GUI,~~ the screen displays:

a breakpoint field that, upon receiving the user input: selects a particular instruction address within the first sequence of instruction addresses shown in a particular processor pipeline stage of the processor pipeline; and displays all instruction addresses of the first sequence along with corresponding stages of the processor pipeline during a clock cycle in which the particular instruction address

is within the particular processor pipeline stage;

a designator for at least one of the instruction addresses to denote that a corresponding designated instruction address will proceed to a succeeding stage in the processor pipeline during a next clock cycle; [[and]]

a non-designator for another ~~one of~~ at least one ~~of the~~ instruction address ~~addresses~~ of the first sequence of instruction addresses to denote that a corresponding non-designated instruction address will not proceed to [[a]] the succeeding stage in the processor pipeline during the next clock cycle; and

an instruction address field that, upon selection by a user, allows the user to move said another at least one instruction address to a different location within the first sequence of instruction addresses, wherein the instruction address in the instruction address field is selected by activating the breakpoint field to freeze a clock cycle and examine instruction addresses within the processor pipeline; and

a scheduler that responds to the moved another at least one instruction address to form a second sequence of instruction addresses that has a higher instruction throughput in the processor pipeline than the first sequence of instruction addresses.

8. (Currently amended) A software development tool stored on ~~a computer-storage medium~~ memory and executable by a computer, the software development tool comprising:

source code represented as a first sequence of instruction addresses;

a graphics rendering engine coupled to receive the first sequence of instruction addresses and

produce a graphical user interface (GUI) window that includes:

a breakpoint field that, upon receiving user input via a pointing device:

selects a particular instruction address within the first sequence of instruction addresses shown in a particular stage of a processor pipeline;

displays all instruction addresses within the first sequence of instruction addresses along with corresponding stages of the processor pipeline during a clock cycle in which the particular instruction address is within the particular stage;

assigns a designator to at least one instruction address of the first sequence of instruction addresses to denote that a corresponding designated instruction will proceed to a succeeding stage in the processor pipeline during a clock cycle succeeding the clock cycle; and

assigns a non-designator to another at least one instruction address of the first sequence of instruction addresses to denote that a corresponding non-designated instruction will not proceed to the succeeding stage in the processor pipeline during the clock cycle succeeding the clock cycle; and

an instruction address field that, upon selection by a user via the pointing device, allows the user to move said another at least one instruction address to a different location within the first sequence of instruction addresses, wherein the instruction address in the instruction address field is selected by activating the breakpoint field to freeze a clock cycle and examine instruction addresses within the processor pipeline; and

a scheduler that responds to the moved [[said]] another at least one instruction address to form a second sequence of instruction addresses that has a higher instruction throughput in the processor pipeline than the first sequence of instruction addresses.

16. (Currently Amended) A method for displaying progression of instruction addresses through a processor pipeline, comprising:

selecting a breakpoint within a breakpoint column of a display screen, via user input at a breakpoint location on the display screen, to select:

an instruction address of a first sequence of instruction addresses representing source code within the same line as the breakpoint[[;]], wherein the instruction address is located in an instruction address field, and

a clock cycle associated with the selected instruction address being in a particular stage within [[the]] a processor pipeline;

designating all instruction addresses of the first sequence of instruction addresses within the processor pipeline that will proceed to a succeeding stage of the processor pipeline; [[and]]

not designating all instruction addresses of the first sequence of instruction addresses within the processor pipeline that will not proceed to [[a]] the succeeding stage of the processor pipeline, wherein upon selection by a user, the instruction addresses not designated to proceed are moved to a different location within the first sequence of instruction addresses; wherein the instruction address in the instruction address field is selected by activating the breakpoint column to freeze a clock cycle and examine instruction addresses within the processor pipeline; and

forming by a scheduler a second sequence of instruction addresses that has a higher instruction throughput in the processor pipeline than the first sequence of instruction addresses, in response to the moved instruction addresses.

***Examiner's Statement of Reason(s) for Allowance***

2. Claims 1 and 3-20 (renumbered as 1-19) are allowed.

3. The following is an examiner's statement of reason s for allowance:

The prior arts of record, taken alone or in combination, fail to teach or fairly suggest at least: a breakpoint field that, upon receiving user input via a pointing device: selects a particular instruction address within the first sequence of instruction addresses shown in a particular stage of a processor pipeline…an instruction address field that, upon selection by a user via the pointing device, allows the user to move said another at least one instruction address to a different location within the first sequence of instruction addresses, wherein the instruction address in the instruction address field is selected by activating the breakpoint field to freeze a clock cycle and examine instruction addresses within the processor pipeline recited in the claims 1, 8, and 16.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to INSUN KANG whose telephone number is (571)272-3724. The examiner can normally be reached on M-R 7:30-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis A. Bullock, Jr. can be reached on 571-272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Insun Kang/
Primary Examiner, Art Unit 2193